GOC-BH440-V1.1

Bluetooth+WIFI Module Hardware Specification

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NOTES:

1. **The module must use ladder steel net, and recommend ladder steel net thickness 0.16--0.20mm. The adaptability of the products is adjusted accordingly.**
2. **Before the use of the module, bake at 60 degrees centigrade and bake for 12 hours.**

Release Record

Version Number	Release Date	Comments
V1.0	2018/08/17	Initial draft
V1.1	2019/01/21	Increase the power on time sequence
V1.2	2019/06/05	Modification temperature
V1.3	2019/08/09	Increase packing methods and performance parameters, Cancel reference design
V1.4	2020/03/03	Update Bluetooth Specification

Contents

1. Introduction

GOC-BH440-V1.1 is a low cost module solution and offers the lowest Goodocom in the industry for smartphones,tablets, and a wide range of other portable devices. The module includes a 2.4 GHz WLAN IEEE 802.11 b/g/n MAC/baseband/radio,Bluetooth 5.1support.In addition, it integrates a power amplifier (PA) that meets the output power requirements of most handheld systems, a low-noise amplifier (LNA) for best-in-class receiver sensitivity, and an internal transmit/receive (iTR) RF switch, further reducing the overall solution cost and printed circuit board area.

The WLAN host interface supports SDIO V2.0 modes, providing a raw data transfer rate up to 200M bps when operating in 4-bit mode at a 50MHz bus frequency. An independent, high-speed UART is provided for the Bluetooth host interface.

This compact module is a total solution for a combination of WiFi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

2. Block Diagram

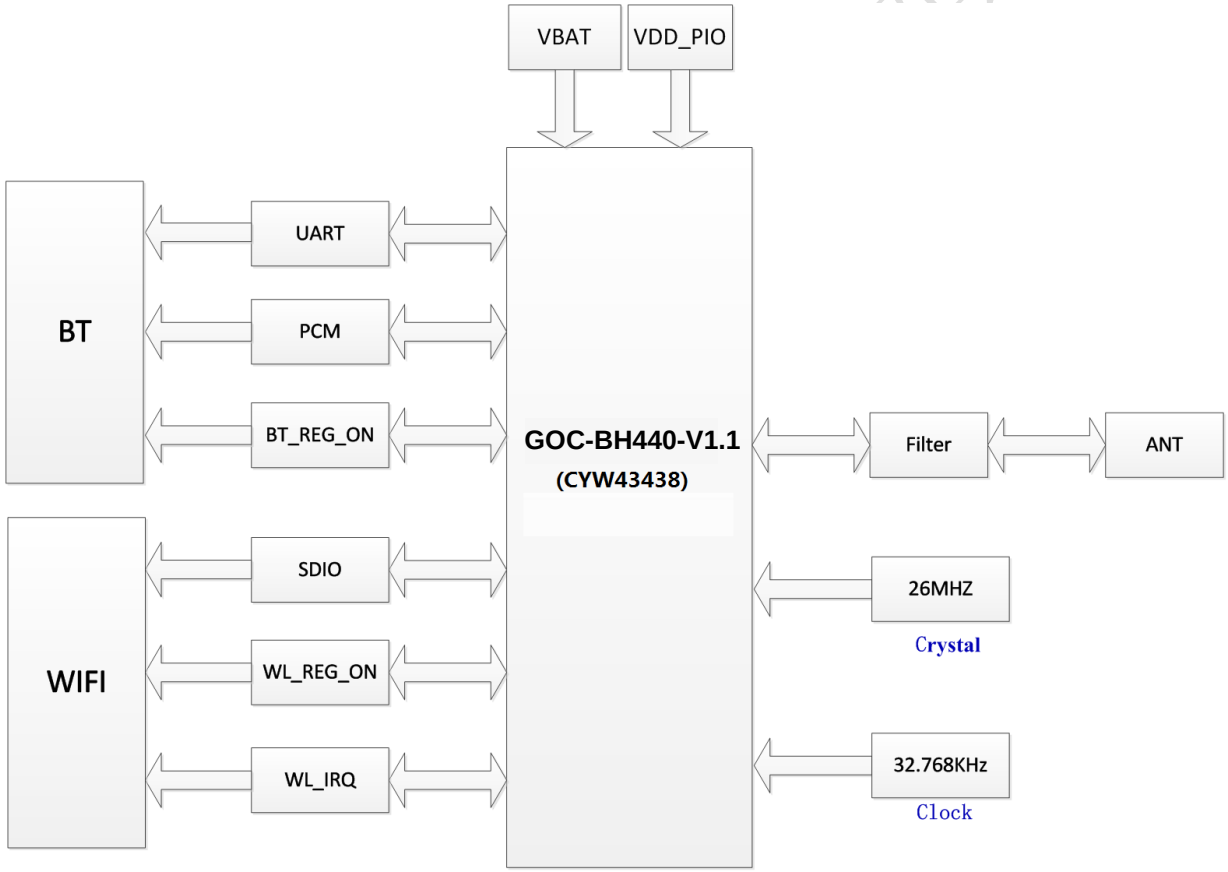


Figure 1: GOC-BH440-V1.1 System Block Diagram

3. Features

3.1 WIFI Features

- Single-band 2.4 GHz IEEE 802.11b/g/n.
- Support for 2.4 GHz Broadcom TurboQAM® data rates (256-QAM) and 20 MHz channel bandwidth.
- Integrated iTR switch supports a single 2.4 GHz antenna shared between WLAN .

- Supports explicit IEEE 802.11n transmit beamforming.
- Tx and Rx Low-density Parity Check (LDPC) support for improved range and power efficiency.
- Supports standard SDIO v2.0 host interfaces.
- Supports Space-Time Block Coding (STBC) in the receiver.
- Integrated ARM Cortex-M3 processor and onchip memory for complete WLAN subsystem functionality, minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field-upgrade with future features.
- OneDriver™ software architecture for easy migration from existing embedded WLAN devices as well as to future devices.
- IEEE 802.11n—Handheld Device Class
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i

The GOC-BH440-V1.1 will support the following future drafts/standards:

- IEEE 802.11r — Fast Roaming (between APs)
- IEEE 802.11k — Resource Management
- IEEE 802.11w — Secure Management Frames
- IEEE 802.11 Extensions:
- IEEE 802.11e QoS Enhancements (as per the WMM® specification is already supported)
- IEEE 802.11i MAC Enhancements
- IEEE 802.11r Fast Roaming Support
- IEEE 802.11k Radio Resource Measurement

The GOC-BH440-V1.1 supports the following security features and proprietary protocols:

- Security:
  - ❒ WEP
  - ❒ WPA™ Personal
  - ❒ WPA2™ Personal
  - ❒ WMM
  - ❒ WMM-PS (U-APSD)
  - ❒ WMM-SA
  - ❒ WAPI
  - ❒ AES (Hardware Accelerator)
  - ❒ TKIP (host-computed)
  - ❒ CKIP (SW Support)
- Proprietary Protocols:
  - ❒ CCXv2
  - ❒ CCXv3
  - ❒ CCXv4
  - ❒ CCXv5
- IEEE 802.15.2 Coexistence Compliance — on silicon solution compliant with IEEE 3-wire requirements

3.2 Bluetooth Features

- Complies with Bluetooth Core Specification Version 5.1 with provisions for supporting future specifications.
- Bluetooth 2.1 + EDR
- Bluetooth 3.0
- Bluetooth Class 2 transmitter operation.

- Bluetooth Low Energy (BLE) support
- Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for
- retransmission of dropped packets.
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference.
- Interface support — Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Automatic frequency detection for standard crystal and TCXO values.

4. Specification

Feature	Description
Model Name	GOC-BH440-V1.1
IC	CYW43438
Bluetooth	
Bluetooth Standard	Bluetooth V5.1
Frequency Band	2402MHz~2480MHz
Interface	UART/PCM
Antenna Reference	50ohm
Modulation	GFSK,π/4DQPSK ,8DPSK,
WIFI	
Standard	IEEE 802.11b/g/n
FrequencyRange	2.412 GHz ~ 2.484 GHz
Interface	SDIO 2.0
Size	17*17 *2.0mm(L*W*H)
Operating temperature	-30℃~+70℃
Storage temperature	-40℃~+125℃
Standby current	25mA
Working current	300mA
Max current	<500mA
VBAT	3.3V
VDD_PIO	1.8V or 3.3V
Humidity	Operating Humidity 60% to 85% Non-Condensing

Table 1: Specifications

5. Pin Diagram and Description

5.1 PIN diagram

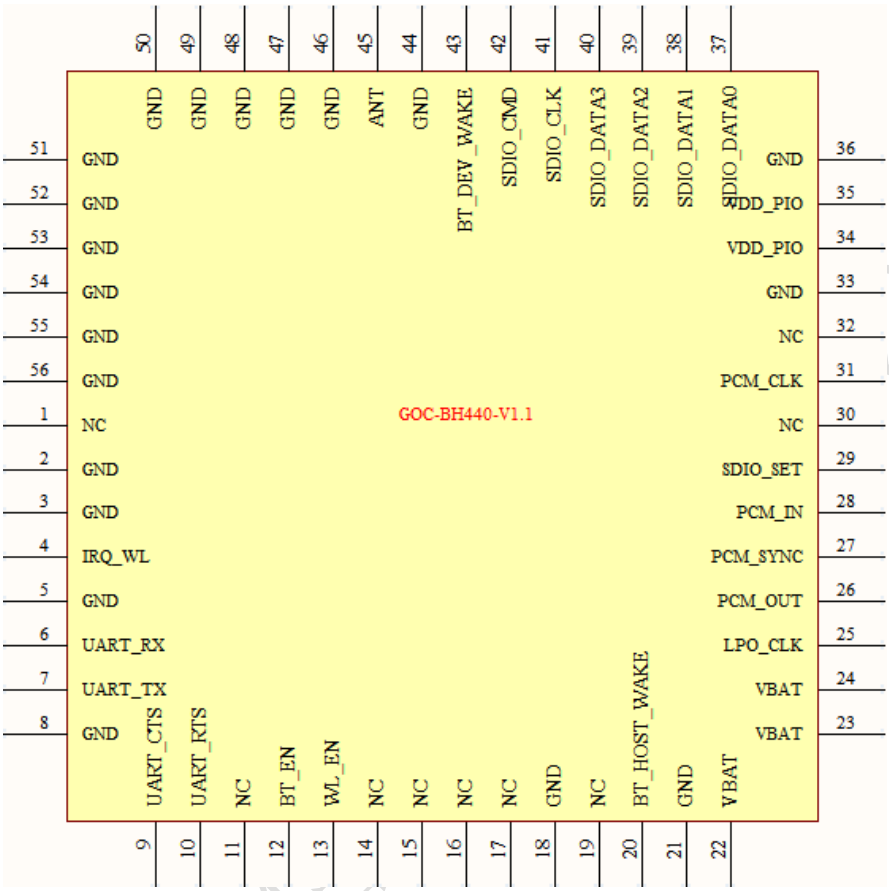


Figure 2: GOC-BH440-V1.1 pin

5.2 Pin Description

Pin	Pin Name	**Type**	Description
1	NC	NC	NC
2	GND	Ground	Ground
3	GND	Ground	Ground
4	IRQ_WL	Input/Output	Programmable GPIO pins. This pin becomes an output pin when it is used as WLAN_HOST_WAKE/out-of-band signal
5	GND	Ground	Ground
6	UART_RX	Input	BT UART Data Input
7	UART_TX	Output	BT UART Data Output

8	GND	Ground	Ground
9	UART_CTS	Input	UART clear-to-send. Active-low clear-to-send signal for the HCIUART interface.
10	UART_RTS	Output	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.
11	NC	NC	NC
12	BT_EN	Input	Used by PMU to power up or power down the internal regulators used by the Bluetooth/FM section. Also, when deasserted, this pin holds the Bluetooth/FM section in reset. This pin has an internal 200 k pull-down resistor that is enabled by default. It can be disabled through programming
13	WL_EN	Input	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 k pull-down resistor that is enabled by default. It can be disabled through programming.
14	NC	NC	NC
15	NC	NC	NC
16	NC	NC	NC
17	NC	NC	NC
18	GND	Ground	Ground
19	NC	NC	NC
20	BT_HOST_WAKE	Input/Output	HOST_WAKE or general-purpose I/O signal
21	GND	Ground	Ground
22	VBAT	POWER	3.3V Supply Voltage
23	VBAT	POWER	3.3V Supply Voltage
24	VBAT	POWER	3.3V Supply Voltage
25	LPO_CLK	Input	External sleep clock input (32.768 kHz). If an external 32.768kHz clock cannot be provided, pull this pin low. However, BLE will be always on and cannot go to deep sleep.
26	PCM_OUT	Output	PCM data output
27	PCM_SYNC	Input/Output	PCM SYNC ; can be master (output) or slave (input)
28	PCM_IN	Input	PCM data input sensing

29	SDIO_SET	Input	SDIO mode selection pin(Reserved)
30	NC	NC	NC
31	PCM_CLK	Input/Output	PCM Clock
32	NC	NC	NC
33	GND	Ground	Ground
34	VDD_PIO	POWER	1.8V~3.3VSupply Voltage
35	VDD_PIO	POWER	1.8V~3.3V Supply Voltage
36	GND	Ground	Ground
37	SDIO_DATA0	Input/Output	SDIO Data Line 0
38	SDIO_DATA1	Input/Output	SDIO Data Line1
39	SDIO_DATA2	Input/Output	SDIO Data Line 2
40	SDIO_DATA3	Input/Output	SDIO Data Line 3
41	SDIO_CLK	Input	SDIO Clock Input
42	SDIO_CMD	Input/Output	SDIO Command
43	BT_DEV_WAKE	Input/Output	DEV_WAKE or general-purpose I/O signal
44	GND	Ground	Ground
45	ANT	RF	WLAN/BT(2.4G)Antenna(Reserved)
46	GND	Ground	Ground
47	GND	Ground	Ground
48	GND	Ground	Ground
49	GND	Ground	Ground
50	GND	Ground	Ground
51	GND	Ground	Ground
52	GND	Ground	Ground
53	GND	Ground	Ground
54	GND	Ground	Ground
55	GND	Ground	Ground

56	GND	Ground	Ground

Table 2: Pin Description

5.3 PCB Layout Footprint

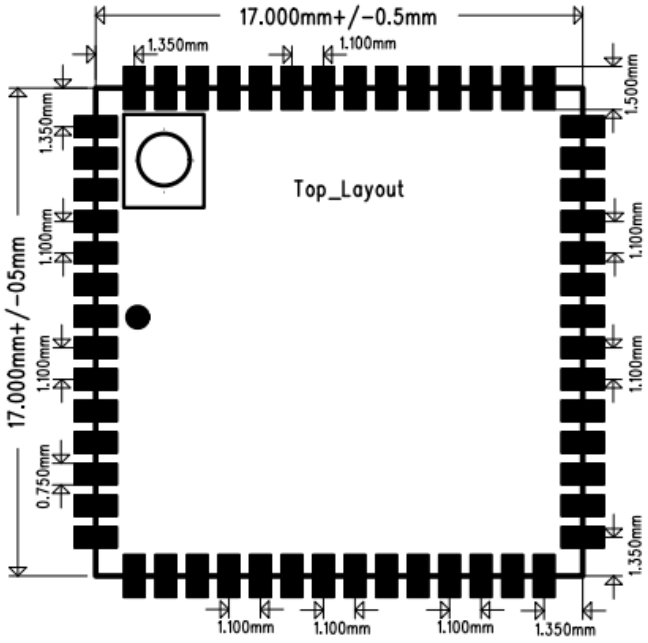


Figure 3: PCB Layout Footprint

5.4 Module Package

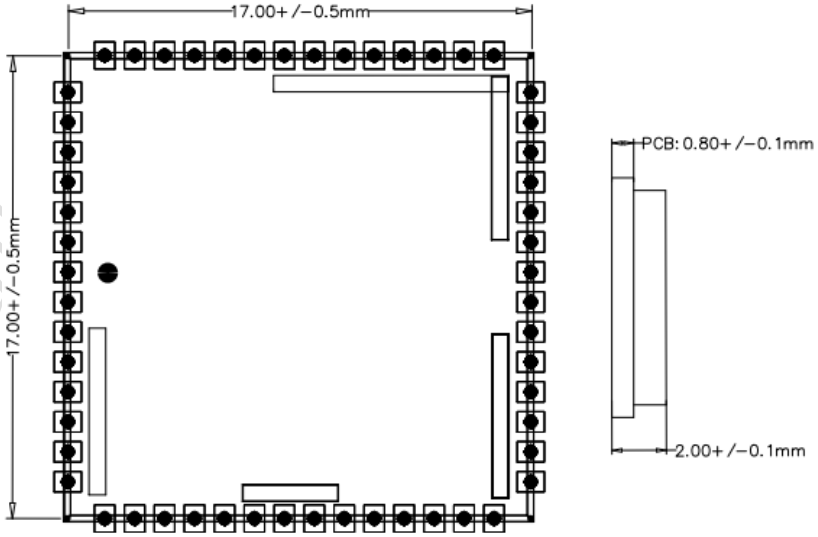


Figure 4: Module Package

6. External LPO_CLK Signal Requirement

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square wave or sine wave	–
Input impedance1	>100k	Ω
	<5	pF
Clock jitter	<10,000	ppm

Note:When power is applied or switched off.

Table 3: External LPO_CLK Signal Requirement

7. Echo Cancellation Principle

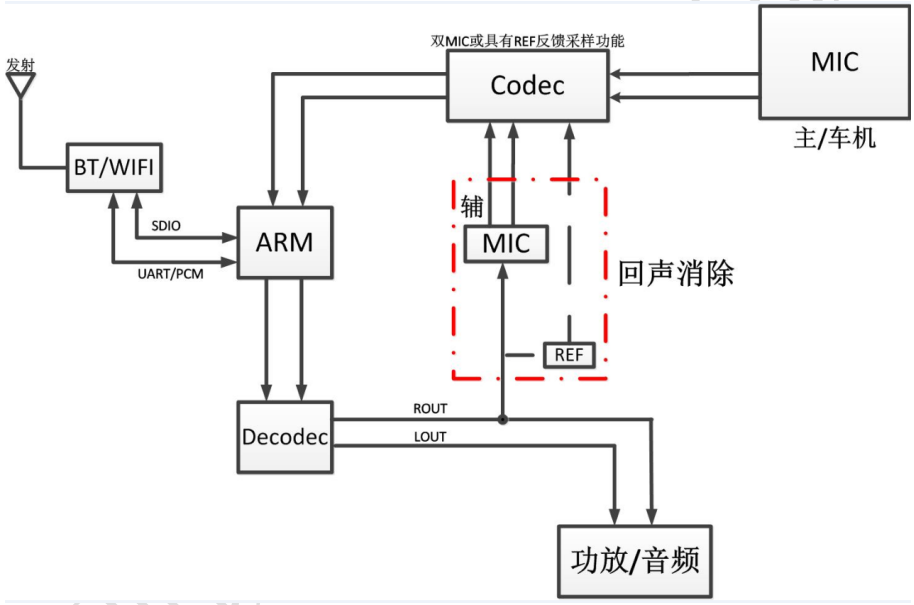


Figure 5: Sound processing flow chart

The left picture is a schematic diagram of the echo cancellation principle. After Decodec decoding of the left and right channel sound, after data sampling and master MIC data comparison, echo cancellation can be processed. The right picture is a reference example, which can be designed according to the actual plan. Flying echo cancellation design, priority to use the echo cancellation design of IFLYTEK.

8. Power-Up Sequence and Timing

8.1 Sequencing of Reset and Regulator Control Signals

The GOC-BH440-V1.1 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states . The timing values indicated are minimum required values; longer delays are also acceptable.

NOTE:

1) The module has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold.Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

2) VBAT and VDDIO should not rise faster than 40 µs. VBAT should be up before or at the same time as VDDIO. VDDIO should not be present first or be held high before VBAT is high.

8.2 Power on sequence for WLAN ON and BT ON

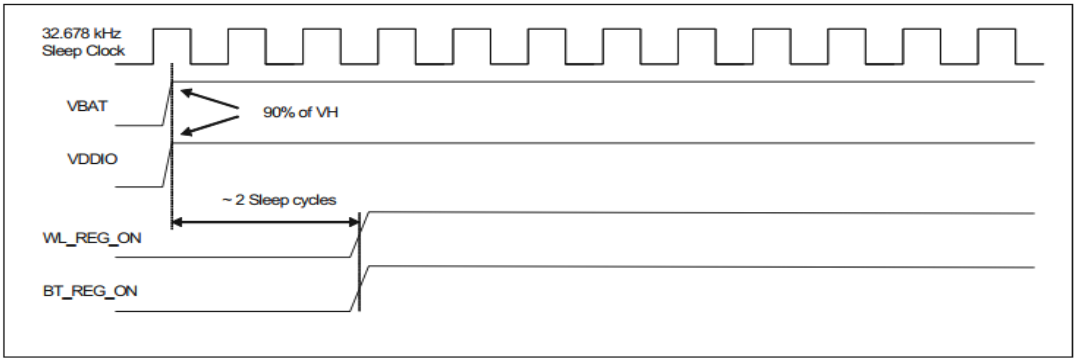


Figure 6: WLAN = ON, Bluetooth = ON

8.3 Power OFF Sequence for WLAN OFF and BT OFF

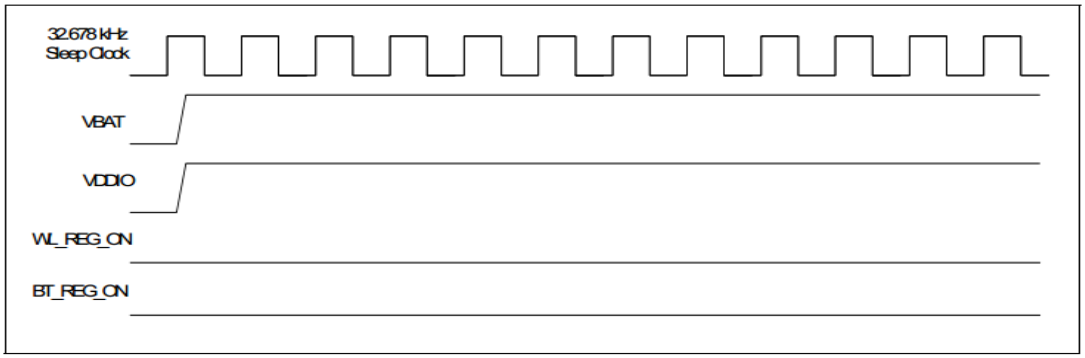


Figure 7: WLAN = OFF, Bluetooth = OFF

8.4 Power On Sequence for WLAN On and BT OFF

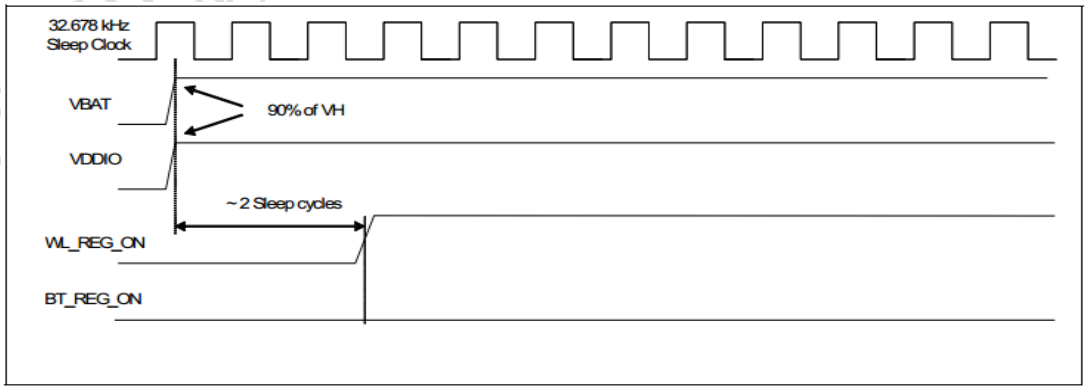


Figure 8: WLAN = ON, Bluetooth = OFF

8.5 Power On Sequence for WLAN OFF and BT On

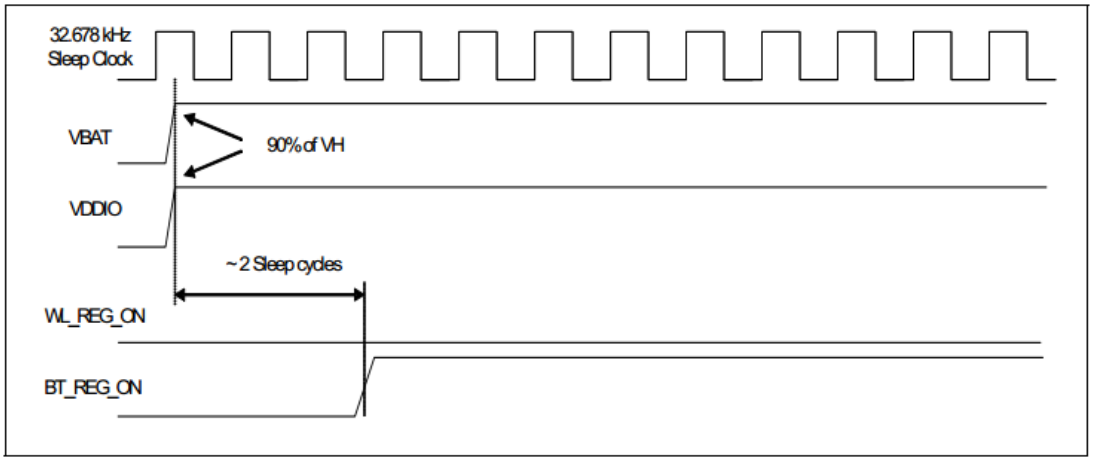


Figure 9: WLAN = OFF, Bluetooth = ON

9. UART Interface

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.1 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The GOC-BH440-V1.1 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The GOC-BH440-V1.1 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16

38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Table 4: Example of Common Baud Rates

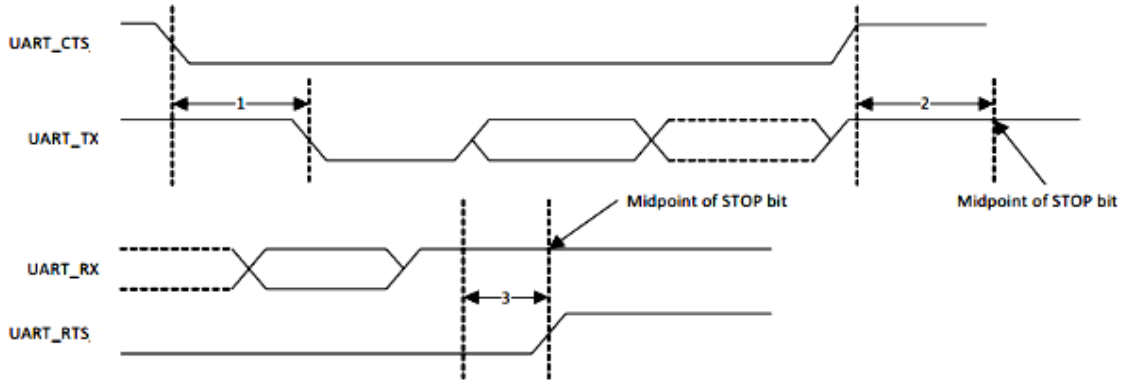


Figure 10: UART Timing

No.	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, UART_CTS low to UART_TX valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS high	–	–	0.5	Bit periods

Table 5: UART Timing Specification

10. SDIO Pin Description

The GOC-BH440-V1.1 WLAN section supports SDIO version 2.0. for both 1-bit (25 Mbps) and 4-bit modes (100 Mbps), as well as highspeed 4-bit mode (50 MHz clocks—200 Mbps). It has the ability to map the interrupt signal on a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force control of the gated clocks from within the WLAN chip is also provided.

SDIO mode is enabled using the strapping option pins.Three functions are supported:

- Function 0 standard SDIO function. The maximum block size is 32 bytes.
- Function 1 backplane function to access the internal System-on-a-Chip (SoC) address space. The maximum block size is 64 bytes.
- Function 2 WLAN function for efficient WLAN packet transfer through DMA. The maximum block size is 512 bytes.

10.1 Signal Connections to SDIO Host

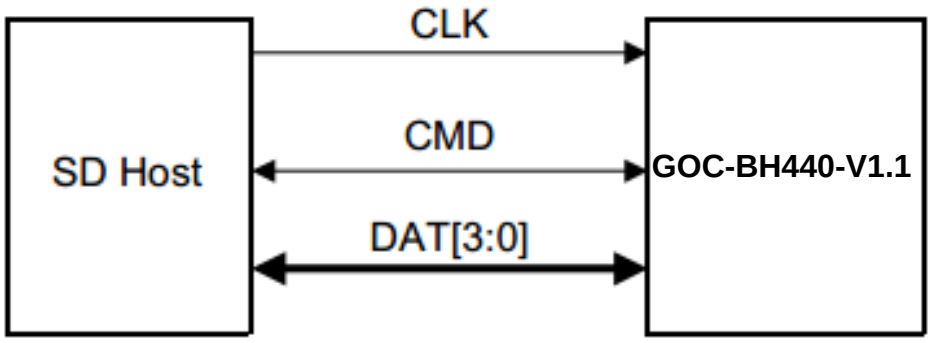
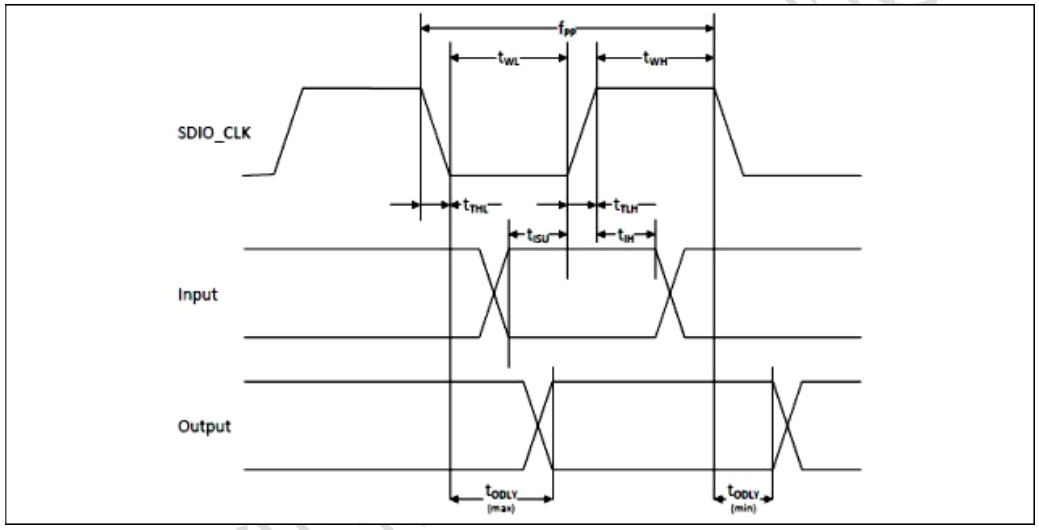


Figure11: Signal Connections to SDIO Host

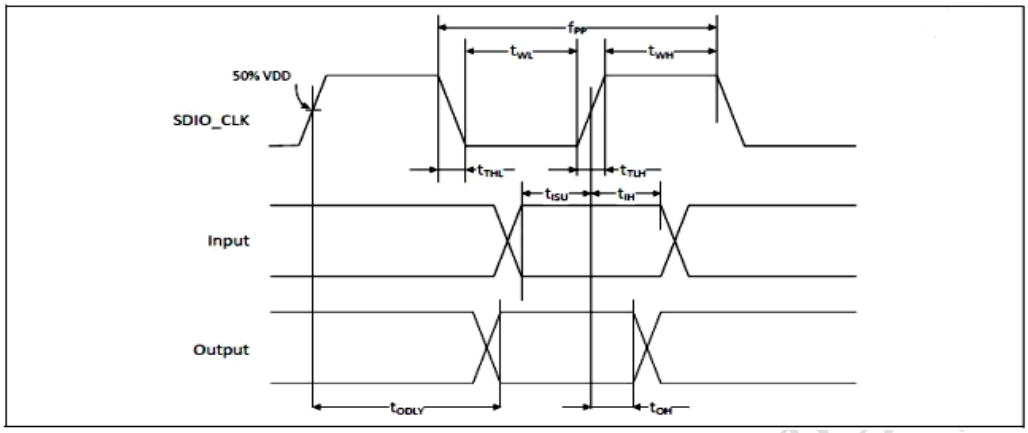
10.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

10.3 SDIO High Speed Mode Timing Diagram

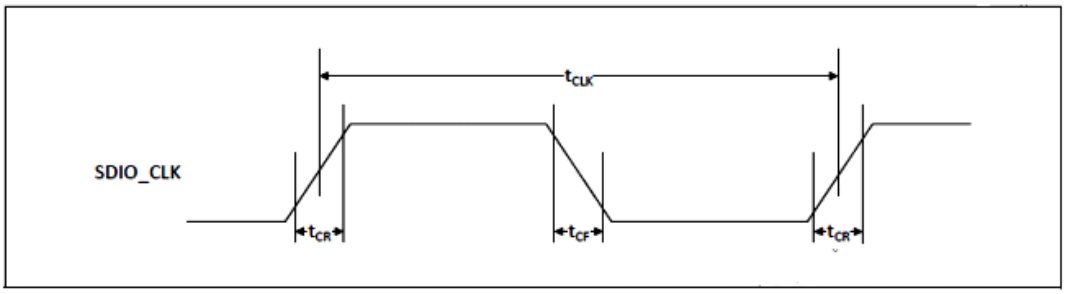


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

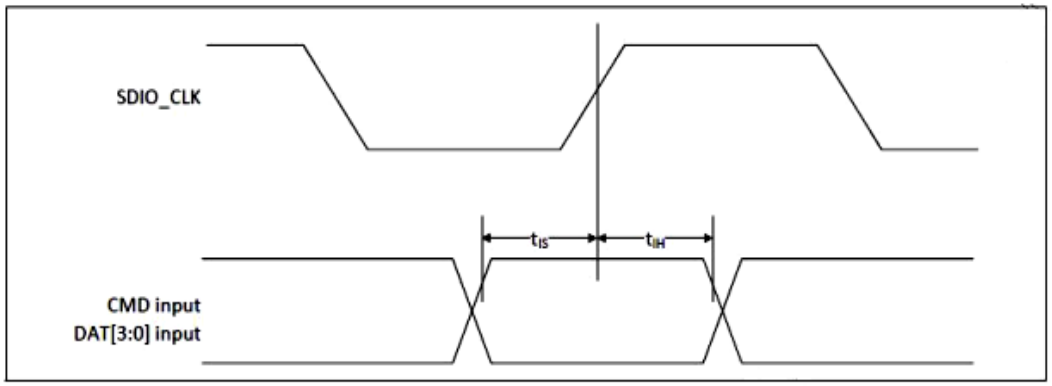
10.4 SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes) :



Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, C_{CARD} = 10 pF
Clock duty	–	30	70	%	–

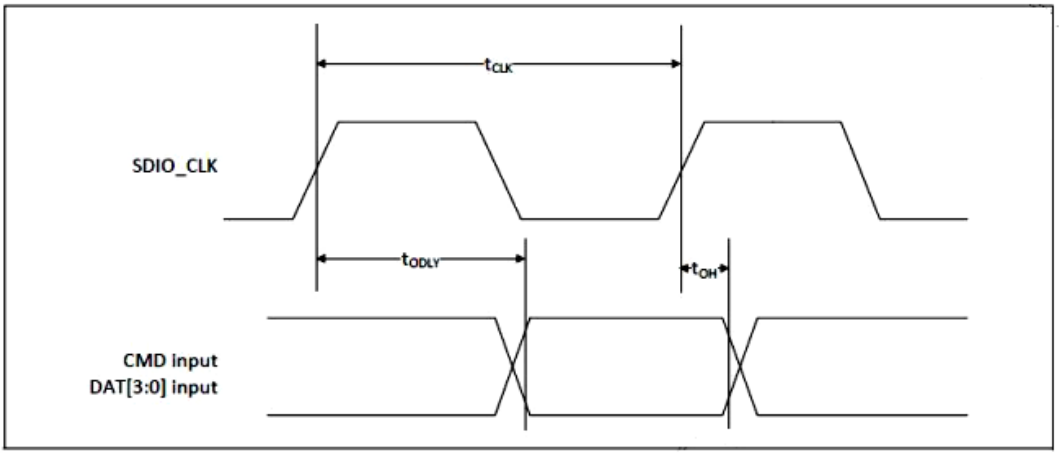
Card Input timing (SDR Modes) :



Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.70[a]	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

a. SDIO 3.0 specification value is 1.40 ns.

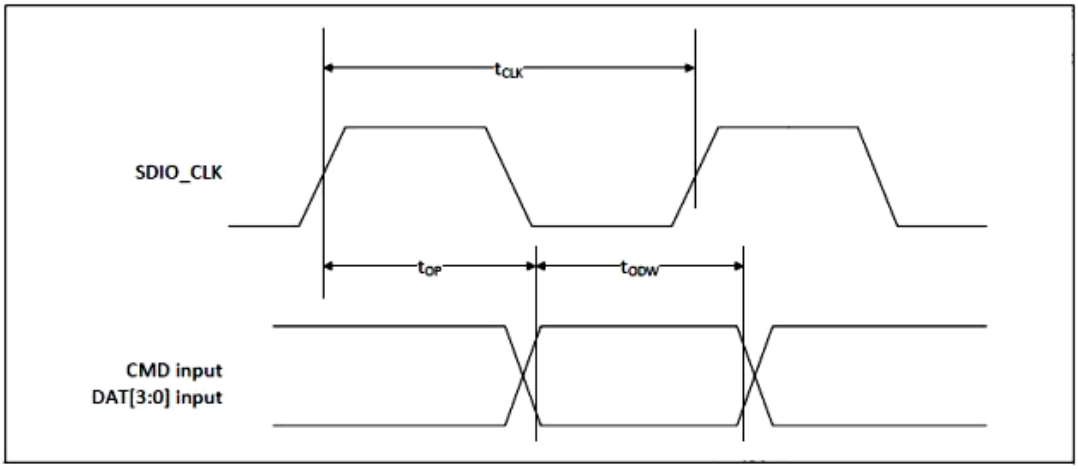
Card output timing (SDR Modes up to 100MHz) :



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.85[a]	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

a. SDIO 3.0 specification value is 7.5 ns.

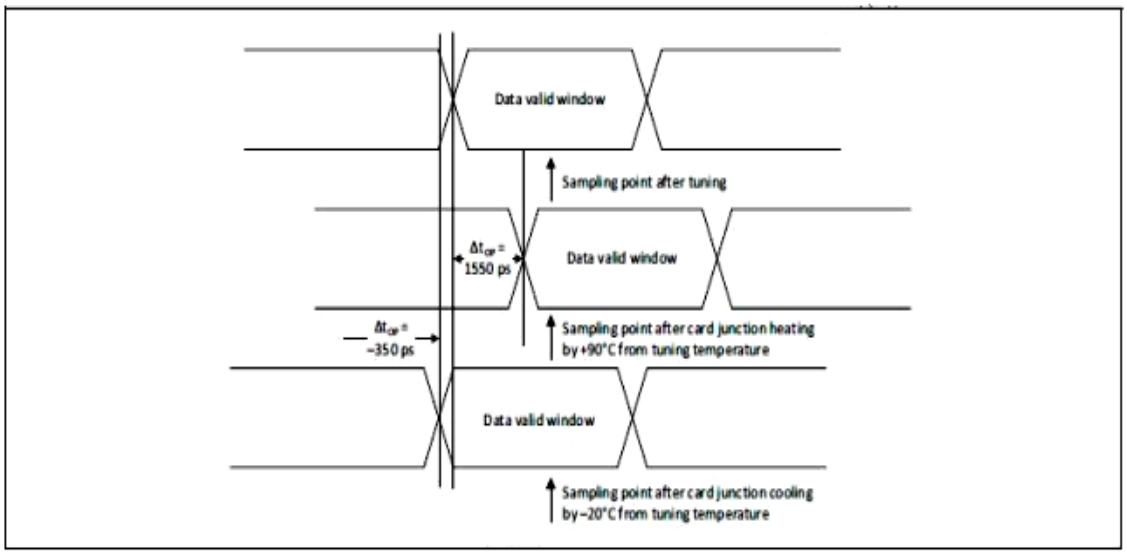
Card output timing (SDR Modes 100MHz to 208MHz) :



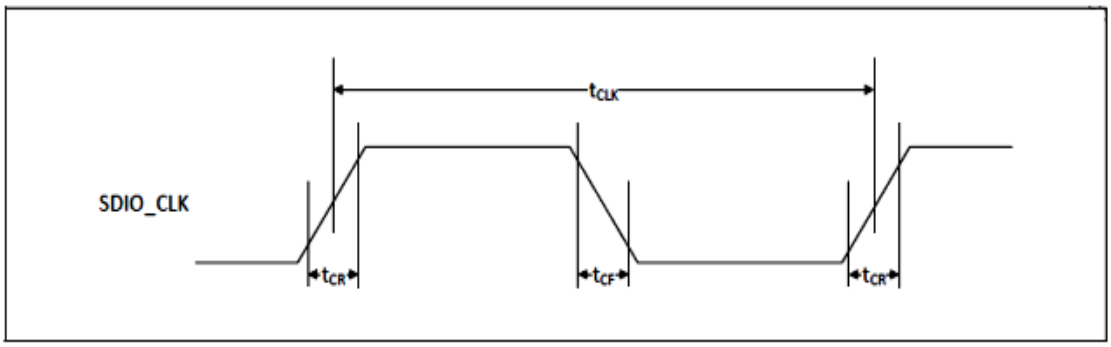
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88 ns @208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = –350 ps for junction temperature of Δt_{OP} = –20 degrees during operation
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = –20 to +125 degrees during operation

Δ*tOP* Consideration for Variable Data Window (SDR 104 Mode)

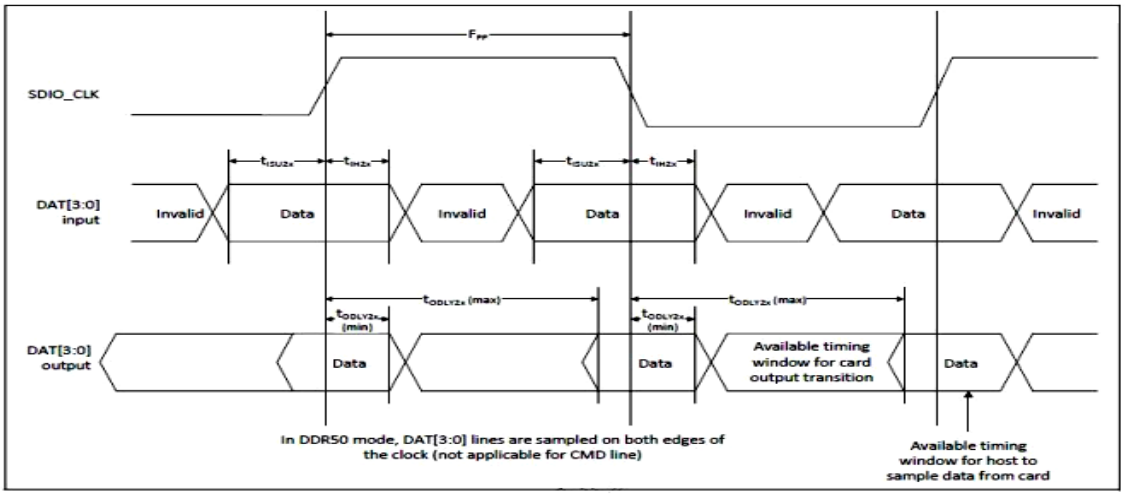


10.5 SDIO Bus Timing Specifications in DDR50 Mode



Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
–	t_{CLK}	20	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty	–	45	55	%	–

Data Timing :



Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.85[a]	ns	C_{CARD} < 25pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15pF (1 Card)

a. SDIO 3.0 specification value is 7.0 ns.

11.PCM Interface

The PCM Interface on the GOC-BH440-V1.1 can connect to linear PCM Codec devices in master or slavemode. In master mode,the GOC-BH440-V1.1 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the GOC-BH440-V1.1.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Slot Mapping

The GOC-BH440-V1.1 supports up to three simultaneous full-duplex SCO or eSCO channels through thePCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The GOC-BH440-V1.1 supports both short- and long-frame synchronization in both master and slave modes. In shortframe synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The GOC-BH440-V1.1 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the GOC-BH440-V1.1 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

PCM Interface Timing

Short Frame Sync, Master Mode

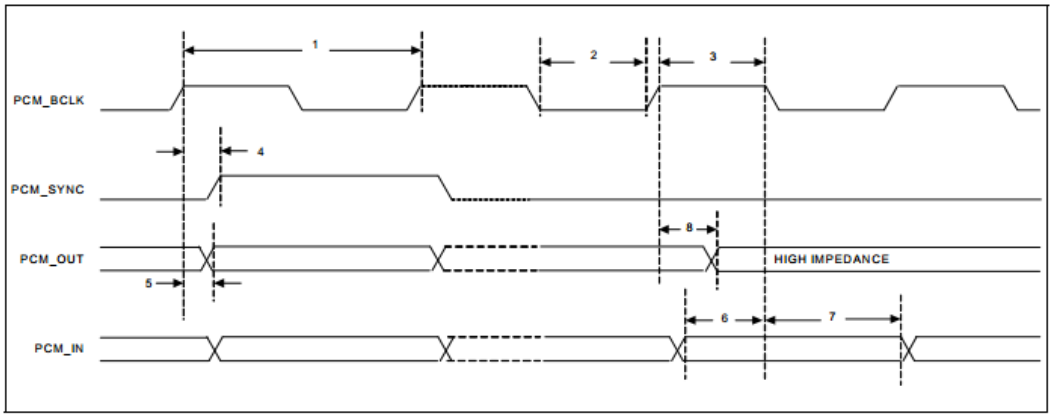


Figure 12: PCM Timing Diagram (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Table6: PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Short Frame Sync, Slave Mode

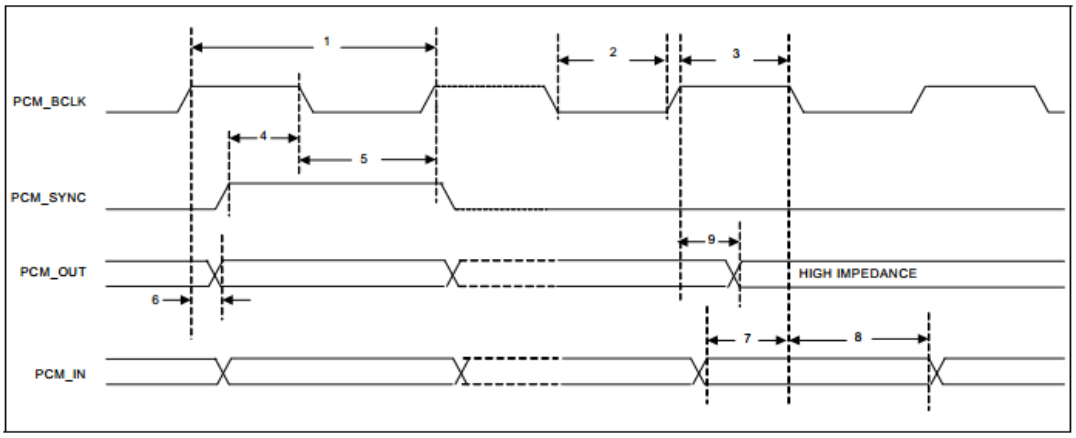


Figure13: PCM Timing Diagram (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Table 7 : PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Long Frame Sync, Master Mode

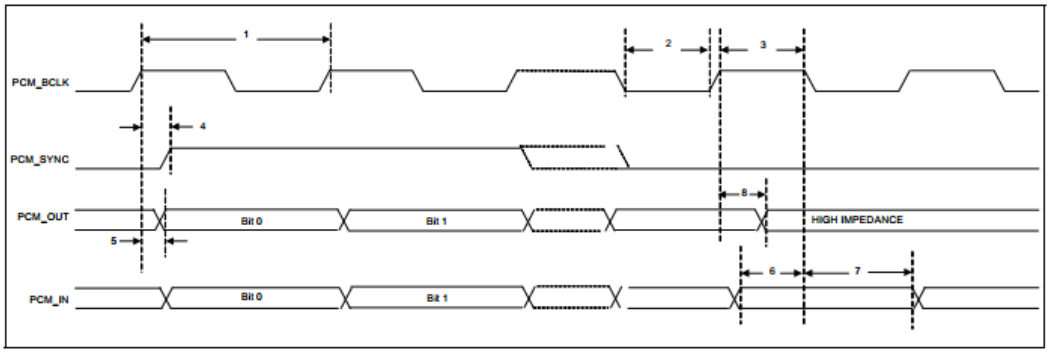


Figure 14: PCM Timing Diagram (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Table 8: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Long Frame Sync, Slave Mode

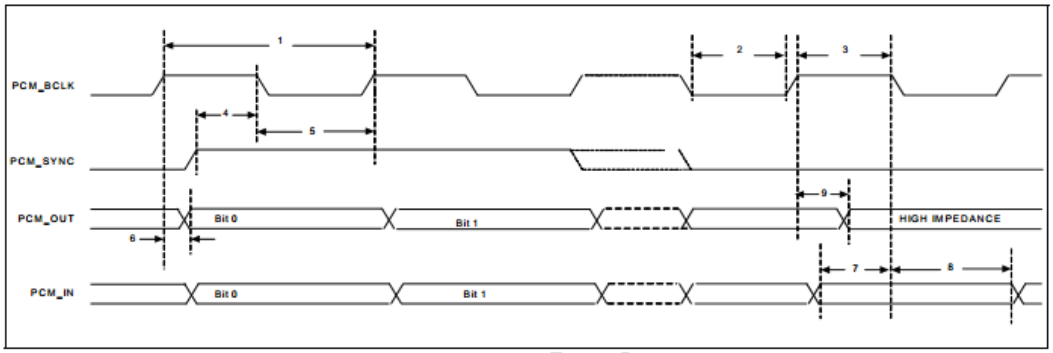


Figure 15: PCM Timing Diagram (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock LOW	41	–	–	ns
3	PCM bit clock HIGH	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Table 8: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Short Frame Sync, Burst Mode

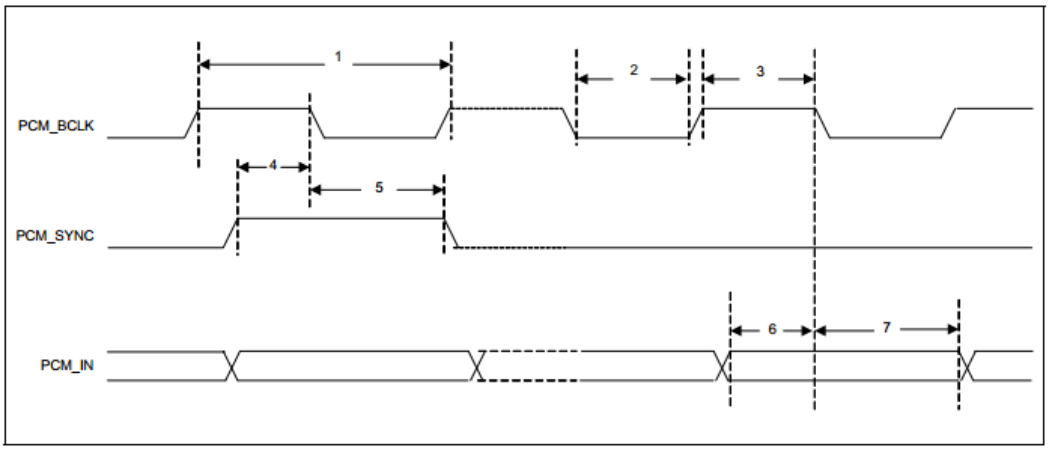


Figure 16: PCM Burst Mode Timing (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Table 9: PCM Burst Mode (Receive Only, Short Frame Sync)

Long Frame Sync, Burst Mode

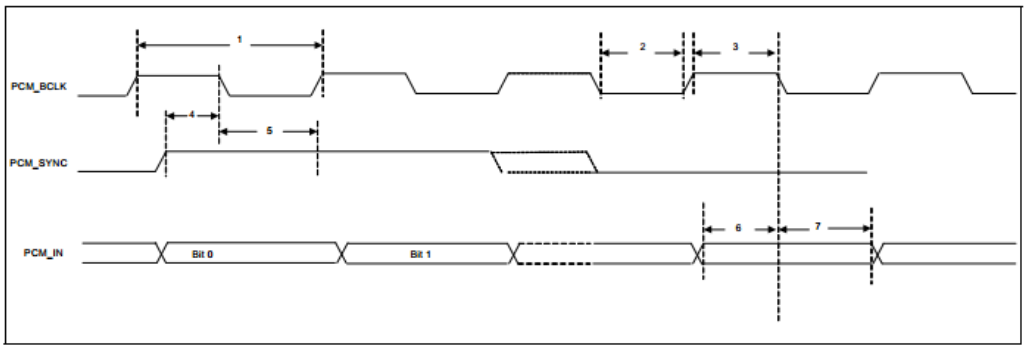


Figure 17: PCM Burst Mode Timing (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Table 10: PCM Burst Mode (Receive Only, Long Frame Sync)

12. Electrical Characteristics

12.1 Recommended Operating Rating

Rated Level	Min	Typical	Max
VBAT	3.0V	3.3V	4.8V
VDD_PIO	1.71V	1.8V	1.89V
	3.16V	3.3V	3.46V

Table 11: Recommended Operating Rating

12.2 Recommended Operating Conditions

Working Condition	Min	Typical	Max
Working Temperature	-30℃	/	+70℃
Storage Temperature	-40℃	/	+125℃

*The module is functional across this range of voltages. However, optimal RF performance specified in the data sheet is guaranteed only for 3.2V <VBAT < 4.8V and -30℃ to +70℃.

Table 12: Recommended Operating Conditions

13. Recommended Reflow Profile

Referred to IPC/JEDEC standard.
Peak Temperature : ≦260℃
Number of Times : 2 times

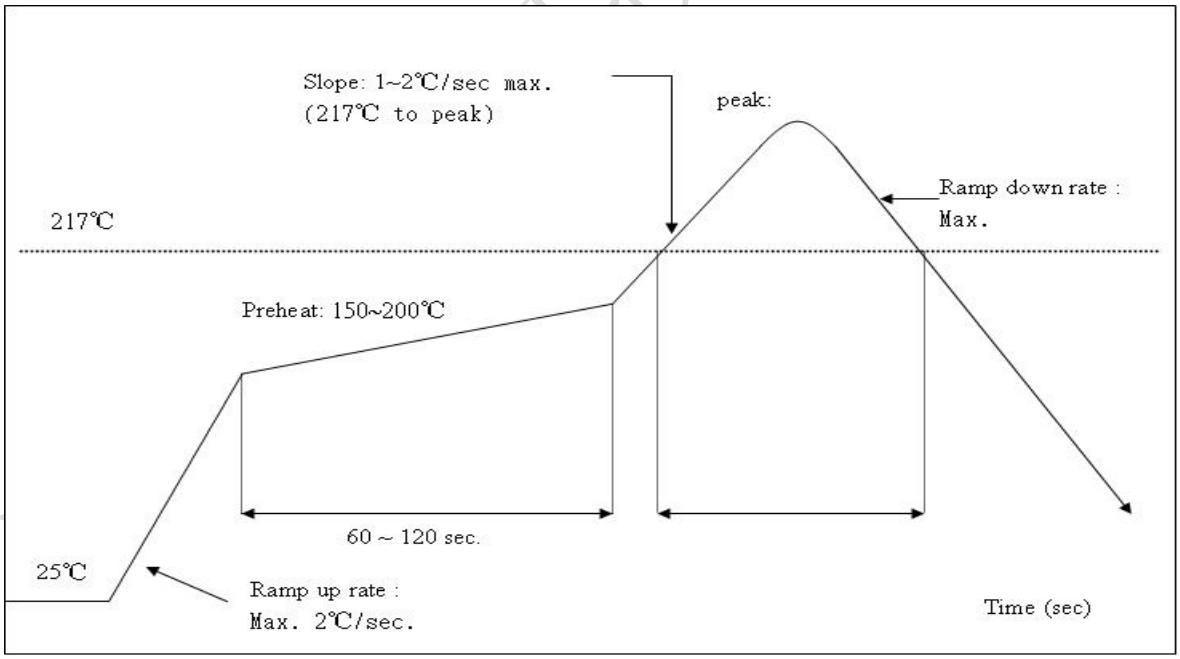


Figure 18 : Solder Reflow Profile

14.PCB Layout Recommendation

14.1 Antenna

Antenna trace impedance should be adjusted to 50ohm.The area above (or under) the RF antenna trace should be free from other traces.

14.2 HCI UART Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA.

UART_RX UART_TX UART_CTS UART_RTS

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

14.3 PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA.

PCM_SYNC PCM_CLK PCM_OUT PCM_IN

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

14.4 Power Trace Lines Layout Guideline

VBAT Trace Width: 30mil

VDD_PIO Trace Width: 25mil

14.5 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to GOC-BH440-V1.1 Module Ground Pads.

Decoupling Capacitors close to GOC-BH440-V1.1 Module Power and Ground Pads.

15. Module Part Number Description

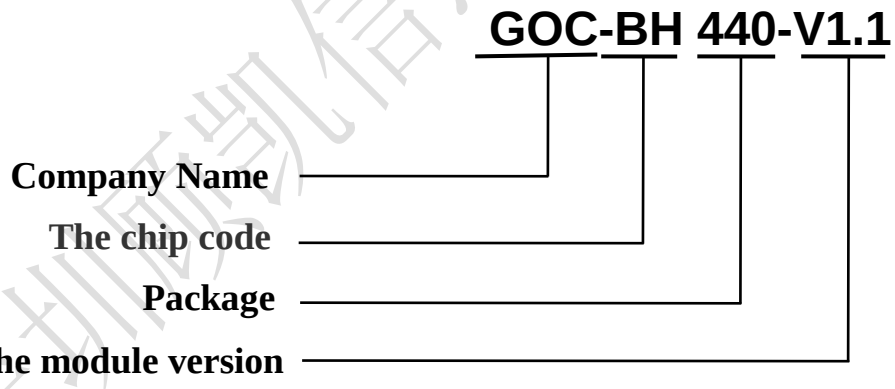


Figure 19: Module Part Number description

For a list of available options and orderable part numbers or for further information on any aspect of this device, please go to www.goodocom.com or contact the GOODOCOM Sales Office nearest to you.

16. Ordering Information

Part Number	Description	Remark
GOC-BH440-V1.1	2.4 GHz single-band WLAN and BT	

Table 13: Ordering information

17.Packaging Information

17.1 Net Weight

The module net weight: 1.3g±0.1g

17.2 Package

72pcs module in one tray 2000pcs modules into one pack 4000pcs Modules One Box Carton size:270mm*275mm*220mm

Tray size:225mm*205mm*7mm

17.3. Storage Requirements

1）Temperature: 22~28℃;

2）Humidity: <70%（RH）;

Vacuum packed and sealed in good condition to ensure 12 months of welding.

17.4. Humidity Sensitive Characteristic

1） MSL: 3 level

2） Once opened, SMT within 168 hours in the condition of temperature: 22~28℃ and humidity<60%(RH).

3） Handling, storage, and processing should follow IPC/JEDECJ-STD-033